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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/443,160	11/19/1999	DAVID L. ISAMAN	130.1012.02	6854

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	17

DATE MAILED: 12/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/443,160	ISAMAN, DAVID L.
	Examiner	Art Unit
	Dam	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20 and 21* is/are allowed.

6)☐ Claim(s) *1-5 and 12-15* is/are rejected.

7)☒ Claim(s) *6-11 and 16-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. Clams 2-21 are presented for examination. Claim 1 has been canceled. Upon further review, and consideration, examiner has applied a new ground of rejection in addition to the previously applied rejection. This is so for the purpose of emphasizing interpretations of the teaching of the prior art which the examiner thinks is important to apply individually in this examination process. Therefore, this is a non-final action to allow the applicant a chance to respond. This outstanding action supercedes the previous action on 06/25/03.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2-5, 12-15 are rejected under 35 U.S.C. 102(a) (b) as being anticipated by Amerson et al. (5,475,823) .

3. As to claims 2,12, the feature of "without computing an external memory address" is interpreted as any method to get to the same memory location as long as the address of that location is not being calculated during the access level. For example, by comparing the load and the store addresses to find the same address, the same address can be used and needs not be calculated. The comparison is a logic operation, not a arithmetic operation, therefore , no calculation involved.

4. Amerson et al. (taught detection of a load that load data from memory location (e.g. see col.1, lines 30-41, col.4, lines 30-37, col.5, lines 16-19) that was previously stored (see the store address accessed the same address as load in col.8, lines 36-43). Amerson did not explicitly characterize his comparison of the load address with store address for determining if the load and store access the same address as "without calculating" the address as claimed. However, by comparing the load and the store addresses to find the same address, the comparison was a logic operation, not a arithmetic operation, therefore , no calculation was being used. Therefore, upon this interpretation, Amerson also did not calculate the address because there was no need for calculating the same address. The subsequent action was that the load instruction in question had a flag set indicating the same address with the store, and the data was forwarded, or loaded (see col.8, lines 37-43).

5. Applicant may have specific method or structure not to or "without calculating the memory address", but it is not being reflected in the claim. Therefore, without further limitations, Amerson is applicable to the claimed invention.

6. As to claims 3, 5, 13, 15, Amerson also detected store in a second location that was previously read (loaded, or read by load instruction. See detection of a store accessing the same address with a load in col.5, lines 29-38, col.6, lines 57-66).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 2-5,12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amerson et al. (5,475,823) in view of Webb, Jr. et al. (6,360,314) .

2. As to claims 2,4,12, 14, Amerson disclosed a system for detecting an instruction [load] that loads data from a first memory location [A1] (see the loading of the memory address in col.1, lines 30-41, see col.4, lines 30-37, col.5, lines 16-19) that was previously stored to (e.g. see col.8, lines 36-41). Amerson did not specifically show the feature of "without computing the external memory address of the first location " as claimed. Instead , it only shows both the load and store referenced the same memory location. However, Webb, Jr. disclosed a system for provide a load data from a recent store instead of having to retrieve the data from a memory upon a match of a comparison result between a load and store address information (e.g. see col.1, lines 60-65, col.2, lines 7-15, col.4, lines 43-48col.6, lines 10-17, col.7, lines 20-26). From the above, it is clear that the load data was provided based on the address comparison, not on a computation of address. In other words, the load data was provided without computing the external memory address because it was provided from the recent store. It would have been obvious to one of ordinary skill in the art to use Webb, Jr. in Amerson for including the feature of without computing the load address as claimed because the use of Webb, Jr. could increase the control ability of Amerson's instruction detector to accept a specific operand data previously stored in memory at a given request, thereby eliminating the address calculating cycle of the memory data , and it could be done by configuring the bypass circuit of Webb, Jr. into

Amerson upon the compare of the load and store addresses to reduce the length of the address cycle, and in doing so, provided a motivation.

3. Amerson is used as a primary reference because it clearly showed a memory location was previously stored (e.g. see the location was accessed by a store in col.8, lines 37-42). Webb Jr. , the secondary reference, although not showing as clear the previously stored location, it is used because it clearly showed the details of the address comparison logic step than Amerson.

4. As to claims 3, 5, 13, 15, Amerson also detected store in a second location that was previously read (loaded, or read by load instruction. See detection of a store accessing the same address with a load in col.5, lines 29-38, col.6, lines 57-66).

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Wing et al. (5,926832) is cited for the basic teaching in the load and store memory access synchronization for eliminating redundant address calculation (e.g. see col.35, lines 51-67, col.36, lines 1-5).

Amerson et al. (5,475,823) and Webb, Jr. et al. (6,360,314) were cited previously , therefore, copies of this patent are not included herein.

Claims 6-11, 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims. None of the prior art of record teaches the detection of the load and store instructions of identical locations in a pipelined microprocessor by examining the symbolic structure of instructions.

Claims 20 , 21 are allowable over the art of record for reciting detailed functional operations of the syntax determination and the respective first and second memory locations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:00 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone numbers for the organization where this application or proceeding is assigned is are:

a) before final 703 746 7239;
b) after final 703 746 7238;
c) Customer Service 703 746 7240.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305 3900. USPTO Web site can be reached at http://www.uspto.gov for general inquiry.

DANIEL H. PAN
PRIMARY EXAMINER
GROUP

21 Century Technologies Inc